PTO: 2000-1342

Japanese Published Unexamined Patent Application No. 4-34942, Published Feb. 5, 1992; Application Filing No. 2-140700, Filed May 30, 1990; Inventor: SATO; Assignee: NEC Corp.

MANUFACTURING METHOD FOR A SEMICONDUCTOR DEVICE

CLAIM:

A method for manufacturing a semiconductor device characterized in containing: a process wherein, after forming a gate oxide film on the surface of a first conductive type semiconductor substrate, a non-crystalline layer is formed on the surface of said semiconductor substrate by ion implantation; a process wherein first conductive type dopants are introduced in the boundary surface between said non-crystalline silicon layer and the monocrystalline region of said semiconductor substrate; a process wherein, after forming a gate electrode from polysilicon, a side-wall is formed from an insulator; and a process wherein a heat treatment is undertaken after said third process is completed.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF USE]

The present invention is related to manufacturing methods for semiconductor devices, and is especially related to methods for forming MOS devices.

[PRIOR ART]

The introduction of dopants in the formation of prior art MOS devices has mainly been accomplished by means of ion implantation.

Along with the miniaturization of device patterns, the joint of the source and drain has become shallow, but in normal ion implantation, tails are generated by channeling, and the joint depth cannot be made shallow.

Double ion implantation methods have been used as a measure for this, for example, as disclosed by C.M. Lim, et. al, in IEEE Electron Device Letters, Vol. 9, No. 11, pp. 594.

Ions are implanted as carriers by the formation of a non-crystalline layer by implanting specified silicon ions.

[PROBLEM OF PRIOR ART TO BE ADDRESSED]

Within the process of forming the source and drain, there is a disadvantage such that, if double ion implantation is effected, the leak current increases in the area of the joint.

Furthermore, when ions are implanted in monocrystalline silicon, the ions disperse in the direction of [illegible], and the effect of this on the development of miniaturization cannot be ignored.

Furthermore, as for the formation of a low dopant concentration layer for the LDD structure of the MOSFET, because of the channeling component, the formation of a shallow joint is very difficult.

The aim of the present invention is to offer a semiconductor device manufacturing method that controls the dopant concentration distribution with high accuracy, and that also controls the size of the leak current.

[MEANS TO ADDRESS SAID PROBLEM]

The semiconductor device manufacturing method of the present invention

comprises a process wherein, after forming a gate oxide film on the surface of a first conductive type semiconductor substrate, a non-crystalline layer is formed on the surface of said semiconductor substrate by ion implantation; a process wherein first conductive type dopants are introduced in the boundary surface of said non-crystalline silicon layer and the monocrystalline region of said semiconductor substrate; a process wherein, after forming a gate electrode from polysilicon, a side-wall is formed from an insulator; and a process wherein a heat treatment is undertaken after said third process is completed.

[FUNCTION]

On the entire surface of a P-type silicon substrate whereupon a field oxide film and a gate oxide film have been initially formed, a group-IV element is ion implanted so as to effect non-crystallization.

Here, the depletion layer does not reach the boundary of the non-crystalline layer.

There is no worry that the gate oxide film, which has an implantation amount of 1 X 10^{14}/cm2, will deteriorate.

Next, because ion implantation of the channel, LDD, source and drain is effected, the problem of the lowered activation rate in a low dose (implantation amount) region is addressed.

Furthermore, because the region wherein dopants have been introduced is non-crystalline, channeling from the introduction of dopants by [illegible] mask does not occur, the problem of tails and of dispersion in a horizontal direction is reduced.

After all ion implantation is completed, because heat treatment is effected all at once, the redistribution of dopants is also [illegible].

[EMBODIMENT]

An embodiment of the present invention will be explained based on figures 1a - 1c.

First, as shown in figure 1a, field oxide film 2 is formed atop P-type silicon substrate 1 by a LOCOS method at a depth of 800nm, and a 7nm gate oxide film 3 is formed by heat oxidation.

Next, germanium ions are implanted at 1 X 10^{14}/cm2 at 150keV and 110keV, so as to form non-crystalline silicon layer 4.

Next, boron ions are implanted at 1 x 10^{13}/cm2 at 110keV, so as to form P+ type embedded layer 5.

Next, boron ions are implanted at 1 x 10^{12} - 1 X 10^{13} cm2 at 30keV, so as to form P-type channel layer 6.

Next, as shown in figure 1b, polysilicon gate electrode 7 is formed, and P ions are implanted at 40 KeV at 1 x 10^{13} -1 x 10^{14} cm2 so as to form an N-type low-concentration layer 8 with an LDD structure.

Next, as shown in figure 1c, an insulated film of PSG is laminated to the entire surface; by etching with an RIE method, a sidewall 9 made of PSG is formed.

Next, P ions are implanted at 70 KeV at 5 x 10^{15} cm2 so as to form N+ type source-drain 10.

After ion implantation has been completed, heat treatment is effected all

at once, causing non-crystalline layer 1 to re-crystallize and effecting the activation of the dopant layer.

Here, short-term lamp annealing is carried out at 900 - 1000 degrees C for 2 - 30 seconds.

Afterwards, an inter-layer insulation film is laminated, contact holes are opened, a metal wiring layer is formed, and the device is completed.

In the present embodiment, germanium ions were used to form non-crystalline silicon layer 4, but silicon ions, tin ions, or other group IV ions are acceptable;

In the present embodiment, non-crystalline layer 4 was formed, then P+ type embedded layer 5 was formed, and then P-type channel layer 6 was formed, but this order may be changed as well.

[EFFECT OF THE INVENTION]

Because the dopant-introduced region is non-crystalline silicon, tails that cause channeling were not observed in the channel layer and the source-drain layer.

By means of lowering the energy used during ion implantation, more shallow dopant layers can be formed.

Without the channeling component, dispersion of dopants in a horizontal direction is decreased as well; it was seen this is beneficial for the formation of fine-pattern devices.

The activation rate within the low-concentration layer is improved as well, and it was seen that a nearly 100% value can be obtained.